

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**APPLICATION FOR LETTERS PATENT**

TITLE:       ***SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE  
INCORPORATING MEMORY CELL TRANSISTOR AND LOGIC  
TRANSISTOR, AND METHOD OF MANUFACTURING THE SAME***

INVENTOR:       Hideaki AOCHI


- 17   Pages Specification
- 13   Claims (pages 18 to 23, including 2 independent claims)
- 18   Figures (9 sheets) (Figs. 1A, 1B, 2A, 2B, 3A, 3B, 4A, 4B, 5A, 5B, 6A, 6B, 7A, 7B, 8A, 8B, 9A and 9B)
- 1   Page Abstract (p. 24)

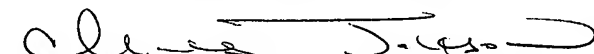
**EXPRESS MAIL**

Mailing Label Number:   EV206803010US

Date of Deposit:       October 31, 2003

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" Service under 37 CFR 1.10 on the date indicated above and is addressed to: **Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

  
(Typed or printed name of person mailing paper or fee)

  
(Signature of person mailing paper or fee)

Edgar H. Haug  
Reg. No. 29,309  
Grace L. Pan  
Reg. No. 39,440  
FROMMER LAWRENCE & HAUG LLP  
745 Fifth Avenue  
New York, New York 10151  
Phone: 212-588-0800  
Fax: 212-588-0500

# TITLE OF THE INVENTION

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCORPORATING  
MEMORY CELL TRANSISTOR AND LOGIC TRANSISTOR, AND METHOD  
OF MANUFACTURING THE SAME

## 5 CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the  
benefit of priority from the prior Japanese Patent  
Application No. 2003-120098, filed April 24, 2003, the  
entire contents of which are incorporated herein by  
10 reference.

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

This invention relates to a semiconductor  
integrated circuit device and a method of manufacturing  
the same, and more particularly, it relates to a  
15 semiconductor integrated circuit device incorporating a  
DRAM in which a memory cell transistor and a logic  
transistor are integrated on the same semiconductor  
substrate, and a method of manufacturing the same.

### 20 2. Description of the Related Art

Generally in a semiconductor integrated circuit  
device incorporating a DRAM, metal silicide is formed  
on a gate electrode by a self-aligned silicidation  
process. It is thus impossible to form a cap  
25 insulating film such as a silicon nitride film on the  
gate electrode, giving a disadvantage that a self-  
aligned contact cannot be used which forms a contact

self-aligningly with the gate electrode of a memory cell transistor.

Therefore, as has been conventionally known, for example, Jpn. Pat. Appln. KOKAI Publication  
5 No. 2000-232076 describes a semiconductor integrated circuit device incorporating a DRAM wherein metal silicide is formed respectively on source and drain regions and on the gate electrode of a logic transistor, and on the gate electrode of the memory  
10 cell transistor so as to achieve high-speed operation, and a sidewall insulating film is formed between the memory cell transistors so as to form a self-aligned contact with the gate electrode of the memory cell transistor.

15 However, gate processing is carried out individually for the memory cell transistor and logic transistor in the one described in the above document, which leads to a disadvantage of complicated manufacturing processes.

20 It is therefore desired that metal silicide is formed respectively on the source and drain regions and on the gate electrode of the logic transistor, and on the gate electrode of the memory cell transistor so as to achieve high-speed operation, and that the self-  
25 aligned contact can be formed with the gate electrode of the memory cell transistor, and further that the gate processing is carried out simultaneously for the

logic transistor and memory cell transistor to reduce the number of manufacturing processes.

#### BRIEF SUMMARY OF THE INVENTION

According to one aspect of the present invention,  
5 there is provided a method of manufacturing a semiconductor integrated circuit device comprises: sequentially forming a gate insulating film, a conductor film containing silicon, and a cap insulating film containing a member capable of selectively etching  
10 a silicon nitride film in each of a first silicon semiconductor region and a second silicon semiconductor region; patterning a laminated film constituted of the cap insulating film and the conductor film to form a gate electrode in each of the first and second silicon semiconductor regions; using the laminated film as a  
15 mask for introducing impurity to selectively introduce the impurity so as to form source and drain diffusion regions in each of the first and second silicon semiconductor regions; forming a first silicon nitride  
20 film on a sidewall of each of the laminated films; forming a second silicon nitride film on an entire surface; depositing a first insulating film on the entire surface, and then leaving the first insulating film between the gate electrodes in the first silicon semiconductor region; depositing a second insulating  
25 film in the second silicon semiconductor region, and then leaving the second insulating film on a sidewall

of each of the laminated films in the second silicon semiconductor region; removing the second silicon nitride film on each of the laminated films and the second silicon nitride film left on a surface of the second silicon semiconductor region; removing the cap insulating film left above each of the gate electrodes; forming a metal silicide film on a surface of the conductor film of each of the gate electrodes and forming a metal silicide film on each surface of the source and drain diffusion regions formed in the second silicon semiconductor region; and depositing a third silicon nitride film on the entire surface, and then leaving the third silicon nitride film on each of the gate electrodes.

According to another aspect of the present invention, there is provided a semiconductor integrated circuit device comprises: a pair of first gate electrodes including a conductor film which are each provided via a gate insulating film in a first silicon semiconductor region; a first diffusion region provided in the first silicon semiconductor region between the pair of first gate electrodes; first metal silicide films provided on upper surfaces of the pair of first gate electrodes respectively; first silicon nitride films provided on the pair of first gate electrodes respectively; second silicon nitride films provided respectively on sidewalls of a laminated film

constituted of the pair of first gate electrodes and  
the first silicon nitride films; a third silicon  
nitride film provided on the second silicon nitride  
film so that the first diffusion region is exposed in a  
5 flat portion positioned between the pair of first gate  
electrodes; a self-aligned contact provided between  
the pair of first gate electrodes and electrically  
connected to the diffusion region; a second gate  
electrode including a conductor film which is formed in  
10 a second silicon semiconductor region via a gate  
insulating film; a pair of second diffusion regions  
formed in the second silicon semiconductor region  
positioned on both surfaces of the second gate  
electrode; a second metal silicide film formed on an  
15 upper surface of the second gate electrode; a fourth  
silicon nitride film provided on the second gate  
electrode; a fifth silicon nitride film provided on a  
sidewall of a laminated film constituted of the second  
gate electrode and the fourth silicon nitride film; a  
20 sixth silicon nitride film provided on the fifth  
silicon nitride film so as to extend onto a portion of  
the surface of the pair of second diffusion regions;  
third metal silicide films provided respectively on the  
surfaces of the pair of second diffusion regions which  
25 are not covered with the sixth silicon nitride film; an  
insulating film provided on the sixth silicon nitride  
film; and a seventh silicon nitride film provided on

the insulating film.

#### BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1A and FIG. 1B are sectional views showing an initial manufacturing process of a method of manufacturing a semiconductor integrated circuit device  
5 according to one embodiment of the invention;

FIG. 2A and FIG. 2B are sectional views showing a manufacturing process following FIG. 1A and FIG. 1B;

FIG. 3A and FIG. 3B are sectional views showing a  
10 manufacturing process following FIG. 2A and FIG. 2B;

FIG. 4A and FIG. 4B are sectional views showing a manufacturing process following FIG. 3A and FIG. 3B;

FIG. 5A and FIG. 5B are sectional views showing a manufacturing process following FIG. 4A and FIG. 4B;

FIG. 6A and FIG. 6B are sectional views showing a  
15 manufacturing process following FIG. 5A and FIG. 5B;

FIG. 7A and FIG. 7B are sectional views showing a manufacturing process following FIG. 6A and FIG. 6B;

FIG. 8A and FIG. 8B are sectional views showing a  
20 manufacturing process following FIG. 7A and FIG. 7B;  
and

FIG. 9A and FIG. 9B are sectional views showing a manufacturing process following FIG. 8A and FIG. 8B.

#### DETAILED DESCRIPTION OF THE INVENTION

25 An embodiment of the invention will hereinafter be described in detail with reference to the drawings.

FIG. 1A, FIG. 1B to FIG. 9A, FIG. 9B are sectional

views sequentially showing manufacturing processes wherein the invention is applied to a semiconductor integrated circuit device in which a DRAM memory cell, and a logic transistor including P-channel and N-channel transistors are integrated on the same semiconductor substrate.

It should be noted that throughout the drawings, A of each drawing shows a region (first region) where the DRAM memory cell is formed, and B of each drawing shows a region (second region) where the logic transistor is formed and shows the manufacture of the N-channel transistor on a left side of the second region and the manufacture of the P-channel transistor on a right side.

First, as shown in FIG. 1A, FIG. 1B, a p-well region 11 is formed on a silicon semiconductor substrate in the first region, and a p-well region 12 and an n-well region 13 are formed on the silicon semiconductor substrate in the second region.

Next, a plurality of trench capacitors 14 are formed at predetermined intervals in the first region by a known method, and in the first and second regions, isolation regions 15 are formed by an STI (shallow trench isolation) process.

The trench capacitors 14 are formed, for example, in the following manner. A deep trench 16 is formed in the p-well region 11 by a selective etching technique.

An n-type impurity is diffused from inside the trench 16 in the p-well region 11 to form an N<sup>+</sup>-type embedded plate electrode 17. A dielectric film 18 for the capacitor is formed on an inner surface of the trench 16. For example, a so-called ON film constituted of a silicon oxide film and a silicon nitride film is utilized as the dielectric film 18. A polycrystalline silicon film 19 doped with the n-type impurity is next embedded about halfway into the trench 16. Further, a silicon oxide film 20 called color oxide is formed on a peripheral surface in an upper portion of the trench 16. A polycrystalline silicon film 21 doped with the n-type impurity is embedded into the vicinity of an upper portion of the trench 16. Subsequently, a shallow trench 22 for the STI is formed, and an insulating film 23 is embedded inside the trench 22, thereby forming the isolation region 15. A shallow trench is formed also in the second region at the same time when the trench 22 is formed, and subsequently an insulating film is embedded in the trench to form the isolation region 15.

Next, as shown in FIG. 2A, FIG. 2B, a gate oxide film 24 is formed on an entire surface by a thermal oxidation method, and then a polycrystalline silicon film into which impurity is introduced is deposited, for example, with a film thickness of 100 nm, on which a thermally-oxidized film, a CVD (chemical vapor

deposition) silicon oxide film 26, and a cap insulating film 27 made of a material such as a silicon oxide film capable of selectively etching the silicon nitride film are sequentially deposited so as to form a laminated film. Subsequently, the laminated film is patterned by RIE (reactive ion etching) using a resist pattern, and a gate electrode 25 made of a polycrystalline silicon film is formed on the first and second regions.

Here, when the gate electrode 25 is formed, a space between the gate electrodes formed in the second region is formed to be wider than a space between the gate electrodes formed in the first region.

Next, as shown in FIG. 3A, FIG. 3B, a sidewall of the patterned laminated film is oxidized, and a silicon nitride film is deposited on the entire surface by the CVD method, and then an etch back by the RIE is carried out, leaving a spacer 28 including the silicon nitride film on the sidewall of the laminated film. Subsequently, the laminated film is used as a mask for introducing the impurity to selectively introduce the impurity, thereby forming diffusion regions which become the source and drain of the transistor in each of the first region and the second region. For example, n-type impurity such as phosphorus is introduced in the first region to form N-type diffusion regions 29, and n-type impurity is also introduced on the left part of the second region to form N-type

diffusion regions 30. At the same time, the entire surface is covered with a protection film, for example, a resist film in the n-well region 13 of the second region. A p-type impurity, for example, boron, is  
5 selectively introduced in a portion of the n-well region 13 of the second region to form P-type diffusion regions 31. At the same time, the entire surface of the first region and the entire surface of the n-well region 13 are covered with protection films, for  
10 example, resist films.

Furthermore, n-type impurity with which the polycrystalline silicon film 21 of the trench capacitor 14 is doped is diffused into the p-well region 11 by heat treatment, to form diffusion regions 32. The  
15 diffusion regions 32 are integrated with the diffusion region 29 that becomes the source and drain of the memory cell transistor.

Next, as shown in FIG. 4A, FIG. 4B, a silicon nitride film 33 is deposited on the entire surface by  
20 CVD with a uniform film thickness, and then a silicon oxide film 34 is deposited by CVD. The thickness of the silicon oxide film 34 is such that a space between the gate electrodes 25 is sufficiently embedded in the first region.

25 Next, as shown in FIG. 5A, FIG. 5B, the silicon oxide film 34 is etched by the RIE until the silicon nitride film 33 on each of the gate electrodes 25 is

exposed. This etching leaves the silicon oxide film 34 in the space between the gate electrodes 25 in the first region.

Subsequently, the entire surface of the first region is protected with a protection film, for example, a resist film, and the silicon oxide film 34 on the second region is removed by wet etching with an HF (hydrogen fluoride)-based solution, and then another silicon oxide film is deposited in the second region by CVD. Further, this silicon oxide film is etched-back by RIE so as to leave spacers 35 made of the silicon oxide film on the sidewall of the laminated film including the gate electrode 25. An upper portion of the silicon nitride film 33 is removed by the etch back during the formation of the spacers 35, so that there are exposed an upper surface of the cap insulating film 27 made of the silicon oxide film on each of the gate electrodes 25 and surfaces of the diffusion regions 30, 31 in the second region.

Next, as shown in FIG. 6A, FIG. 6B, the cap insulating films 27, thermal oxide films and CVD silicon oxide films 26 on the gate electrodes 25 are sequentially removed by the selective etching method, and thus a surface of each of the gate electrodes 25 is exposed. Subsequently, a self-aligned silicidation process is carried out, so that a metal silicide film 36 is formed on an upper surface of each of the gate

electrodes 25, and the metal silicide films 36 are formed on upper surfaces of the diffusion regions 30, 31 in the second region. More specifically, a metal, for example, a cobalt film for forming silicide is deposited on the entire surface with a film thickness of about 30 nm by sputtering, and then a heat treatment at about 550°C is applied so as to form cobalt silicide on the silicon layer and on the polycrystalline silicon layer contacting the cobalt film.

Next, as shown in FIG. 7A, FIG. 7B, a silicon nitride film 37 is deposited by CVD so that the space between the gate electrodes 25 is completely filled.

Next, as shown in FIG. 8A, FIG. 8B, the silicon nitride film 37 is etched-back by RIE, leaving the silicon nitride film 37 self-aligned on each of the gate electrodes 25 in the first region. In addition, the silicon nitride film 37 is left on the sidewall of each of the gate electrodes 25 in the second region. It should be noted that the treatment needs to be carried out at a low temperature such that the metal silicide film 36 does not agglutinate, during deposition and etching of the silicon nitride film 37.

Subsequently, as shown in FIG. 9A, FIG. 9B, an interlayer insulation film 38 made of a silicon oxide film is deposited on the entire surface, and contact holes are opened in the interlayer insulation film 38 by the selective etching technique which is dependent

on a condition under which the silicon oxide film is etched, and thus contacts (connection contacts) are formed.

More specifically, in the first region, the selective etching is applied to the interlayer insulation film 38 and silicon oxide film 34 so as to open a contact hole 39 that reaches a surface of the diffusion region 29 positioned between a pair of gate electrodes 25 adjacent to each other, and then a metal, for example, tungsten is embedded inside the contact hole 39 and flattened, thereby forming a contact 40. When the contact hole 39 is opened, the silicon nitride film 37 is present on the pair of gate electrodes 25, and the silicon nitride films 28, 33 are present on the sidewalls of the pair of gate electrodes 25. These silicon nitride films 37, 28, 33 are difficult to etch as compared with the silicon oxide film during the selective etching. Therefore, owing to the presence of the silicon nitride films 37, 28, 33, the contact hole 39 is opened self-aligningly with the gate electrode 25, so that the contact 40 becomes a self-aligned contact.

In the second region, the selective etching is applied to the interlayer insulation film 38 so as to open contact holes 41 that reach surfaces of the diffusion regions 30, 31 positioned on both sides of each of the gate electrodes 25, and then tungsten is

embedded inside the contact holes 41 and flattened, thereby forming contacts 42.

5 In the second region, the metal silicide film 36 is formed respectively on the diffusion regions 30, 31 which become the source and drain and on the gate electrode 25 of the logic transistor, and on the gate electrode 25 of the memory cell transistor. As a result, resistance of the source, drain and gate electrodes can be reduced and high-speed operation can  
10 be achieved.

Furthermore, in the first region, the contact 40 is formed self-aligningly with the gate electrode 25 of the memory cell transistor.

15 In addition, gate processing is carried out simultaneously for the logic transistor and memory cell transistor, thereby making it possible to reduce the number of manufacturing processes.

20 It should be noted that, in the p-well region 11 shown in FIG. 9A, there are formed the pair of gate electrodes (first gate electrodes) 25 each made of a silicon conductor film which is provided via the gate oxide film (gate insulating film) 24; the N-type diffusion region (first diffusion region) 29 provided in the p-well region 11 between the pair of gate  
25 electrodes 25; the metal silicide films 36 (first metal silicide films) provided respectively on the upper surfaces of the pair of gate electrodes 25; the silicon

nitride films (first silicon nitride films) 37 provided  
on the pair of gate electrodes 25 respectively; the  
silicon nitride films (second silicon nitride films) 28  
provided respectively on the sidewalls of the laminated  
5 film constituted of the pair of gate electrodes 25 and  
the silicon nitride films 37; the silicon nitride film  
(third silicon nitride film) 33 provided on the silicon  
nitride film 28 so that the first diffusion region is  
exposed in a flat portion positioned between the pair  
10 of gate electrodes 25; and the self-aligned contact 40  
provided between the pair of gate electrodes 25 and  
electrically connected to the diffusion region 29.

In the p- and n-well regions 12, 13 shown in  
FIG. 9B, there are formed the gate electrode (second  
15 gate electrode) 25 made of a silicon conductor film  
which is provided via the gate oxide film (gate  
insulating film) 24; the pair of N-type or P-type  
diffusion regions (second diffusion regions) 30, 31  
formed in the p- or n-well regions 12, 13 positioned on  
20 both surfaces of the gate electrode 25; the metal  
silicide film (second metal silicide film) 36 formed on  
the upper surface of the gate electrode 25; the silicon  
nitride film (fourth silicon nitride film) 37 provided  
on the gate electrode 25; the silicon nitride film  
25 (fifth silicon nitride film) 28 provided on the  
sidewall of the laminated film constituted of the gate  
electrode 25 and the silicon nitride film 37; the

silicon nitride film (sixth silicon nitride film) 33 provided on the silicon nitride film 28 so as to extend onto a portion of the surfaces of the diffusion regions 30, 31; the metal silicide films (third metal silicide films) 36 provided respectively on the surfaces of the diffusion regions 30 and 31 which are not covered with the silicon nitride film 33; the spacer (insulating film) 35 made of a silicon oxide film which is provided on the silicon nitride film 33; and the silicon nitride film (seventh silicon nitride film) 37 provided on the spacer 35.

In the semiconductor integrated circuit device thus configured, the metal silicide films 36 are formed respectively on the diffusion regions 30, 31 which become the source and drain and on the gate electrode 25 of the logic transistor, and on the gate electrode 25 of the memory cell transistor, so that the resistance of the source, drain and gate electrode can be reduced and high-speed operation can be achieved.

Furthermore, the contact 40 self-aligning with the gate electrode 25 of the memory cell transistor is formed.

It should be noted that the cobalt silicide film is used as the metal silicide film 36 in the embodiment described above, but a titanium silicide film, molybdenum silicide film or the like may be used instead thereof.

Furthermore, a case where the trench capacitor is formed in the first region has been described in connection with the above embodiment, but a stack capacitor may be formed instead.

5           Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various  
10           modifications may be made without departing from the spirit or scope of the general invention concept as defined by the appended claims and their equivalents.